DESIGN OF LOW POWER HIGH PERFORMANCE STATIC LOGIC BINARY COMPARATOR

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***Abstract*-Binary comparison is a fundamental operation for most digital systems. Comparator is a very basic component used to detect whether the input is equal to or larger than or less than the other input. There are several approaches for designing comparators each with different operating speed, power consumption and circuit complexity. This project describes a new architecture for designing a 64-bit static low-power high-performance binary comparator based on pass transistor logic. Pass transistor logic reduces the number of transistors compared to CMOS logic style. For 130nm technology, the power is reduced for static logic binary comparator when compared to the existing designs.**

***Keywords*: Binary Comparator, Pass transistor logic, CMOS logic**

I. INTRODUCTION

A binary comparator have always been an important block in an arithmetic logic unit and also has extensive applications in many digital systems. The comparator is a very basic and useful arithmetic component of digital systems. Digital Comparator also called "Magnitude Comparator" is a combinational circuit that compares two input binary quantities (A and B) and generates outputs to indicate whether one input is equal to or less than or greater than the other inputs.

The multiple-input-multiple-output (MIMO) technology has increased the need for low power high-performance comparators, because MIMO decoding algorithm requires extensive iterations of binary comparison [6], [10]. T.H. Kim et al. proposed a new K-best detection method that can realize a small-area and low-energy MIMO detector. To reduce the complexity, relaxed tree expansion is used. Also proposed an efficient pipeline scheduling called early forwarding to reduce the overall processing latency and number of registers. Power consumption is reduced by minimizing the number of registers.

In [4] and [7] two single-cycle two-phase clocking architectures are presented. C.H. Huang et al. proposed power-efficient CMOS comparator based on the priority encoder algorithm. In this, priority-encoding function and subsequent AND function are merged as an Magnitude Decision Module (MDM). Such a design not only improves the operating speed due to the reduced logic path, but also makes the circuit compact and power efficient because fewer transistors are used. To efficiently shorten the critical path multilevel look-ahead technique is used.

H.M. Lam et al. presented a parallel MSB checking method instead of the traditional priority-encoding based comparison algorithm. In this, fast dynamic NOR gates are used instead of high fan-in NAND gates which results in significant improvement in performance. In order to further increase the speed, a modification of the MSB checking algorithm used in [7] was proposed in [8], where a MUX-based structure specifically designed for high fan-in comparators. The architecture is based on two comparator structure and a dynamic MUX is used instead of a comparator in the second stage of the structure. To achieve high performance, dynamic logic with phase pipelining is used.

The fast dynamic MUX significantly improves the overall delay of the high fan-in comparators. To avoid race problem for cascading the dynamic gate, the dynamic priority encoder use the ―equal‖ signal instead of the ―unequal‖ signal to enable/disable the lower bit priority encoder. Static logic is used for the priority encoder. Because of the use of static logic, the race problem is not considered for cascading the dynamic gate and use a dynamic NOR gate instead of using a dynamic AND gate. The number of transistors on the critical path is less than that of the priority encoder. At the same time, the delay is reduced by using the dynamic NOR gate to disable the lower bit group.

In 2007, Kim and Yoo [5] proposed a new compact high performance and area efficient digital comparator with bitwise competition logic (BCL) which has no arithmetic computation. It compares two integer numbers using the location of the first 1 from the MSB, without arithmetic computations. In BCL, each segment is operated in parallel. This design achieves the lowest number of transistors count. BCL comparator reduces propagation delay and area compared to other comparators. An important feature of the binary comparator is that its architecture can be easily implemented by using both full-custom and standard-cell-based design approaches. High-speed adders, such as the carry look-ahead, can drastically increase the hardware complexity.

F. Frustaci and S. Perri proposed high-speed single clock cycle binary comparator based on ultra-low-power

high-speed parallel-prefix algorithm. This allows to achieve results in a very low power consumption. This achieves reduction in energy dissipation and improvement in speed.

Designs in [2], [4], [5] and [9] may not be suitable for static logic implementation because of the tall transistor stack height.

II. EXISTING COMPARATOR DESIGNS

A brief description of existing comparator designs are provided here.

A. Priority-Encoding-Based Comparator

Let the two inputs of the comparator be A and B, both with n bits counted from bit 0 to bit n-1. The binary variable A_{big} (B_{big}) denotes that A (B) is larger than B (A). Another binary signal EQUAL indicates A is equal to B. A 4-bit numerical example is used to demonstrate the design concept of the comparator.

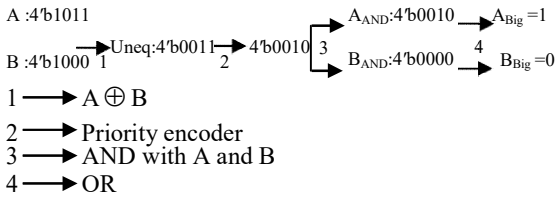


Figure 1. Four-bit numerical priority encoder algorithm [4]

B. Bitwise Competition Logic-Based comparator

The size of two long binary numbers can be easily compared by identifying the location of the first one from the MSB: The one that has the first one in the MSB is the larger. In case that the locations of the first one are the same in both numbers, the decision is moved to next lower bit where only one input has 1 in that bit position.
Consider two 4-bit inputs

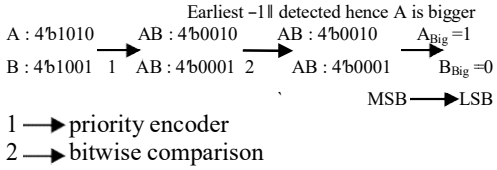


Figure 2. Four-bit numerical BCL algorithm [8]

Steps involved in this algorithm:

Step 1. Input A and B pre-encoded into A^* and B^* each.
Step 2. Bit comparison is performed (initial=MSB)
Step 3. If 1 is detected, that input is decided to be the larger.
Step 4. If no 1 is detected, move to next lower bit and repeat from Step 2 until find first1.

reduced switching activity of the internal nodes which

III. PROPOSED 64-BIT RADIX-2 TREE STRUCTURE BASED COMPARATOR

Digital or Binary Comparators are made up from standard AND, OR and NOT gates that compare the digital signals present at their input terminals and produce an output depending upon the condition of those inputs. There are several approaches to designing comparators each with different operating speed, size, power consumption, and circuit complexity.

The proposed tree-structure based comparator is inspired by the fact that G (generate) and P (propagate) signals can be designed for binary comparisons, similar to the G and P signals for binary additions.

A. Basic Design Principle

A two 2-bit binary number (A_1A_0 and B_1B_0) comparison can be given by the equation

$$B_{Big} = \overline{A}_1 B_1 + \left(\overline{A \oplus B}_1\right)\left(\overline{A}_0 B_0\right) \quad (1)$$

$$EQ = \left(\overline{A \oplus B}_1\right)\left(\overline{A \oplus B}_0\right) \quad (2)$$

If B > A, then — B_{Big}, EQ ‖ is — 1,0. ‖ — B_{Big}, EQ ‖ is — 0,0 ‖ If A > B and — 0,1 ‖ if A=B. Consider the following carry generation:

$$C_{out} = AB + (A \oplus B)C_{in} = G + PC_{in} \quad (3)$$

where A and B are the binary inputs, C_{in} is the carry input, C_{out} is the carry output, and G and P are the generate and propagate signals, respectively. Comparing (1) and (3), one can define $G_1 = \overline{A_1}B_1$, $EQ_1 = \overline{A_1 \oplus B_1}$ and $C_{in} = \overline{A_0}B_0$ for B_{Big} . Here C_{in} is taken as G_0. Equation (1) may not be suitable for high-performance operation when implementing with static logic, due to the tall transistor height and a complicated XNOR gate. An encoding scheme is employed to mitigate this problem.
The encoding equation is given as

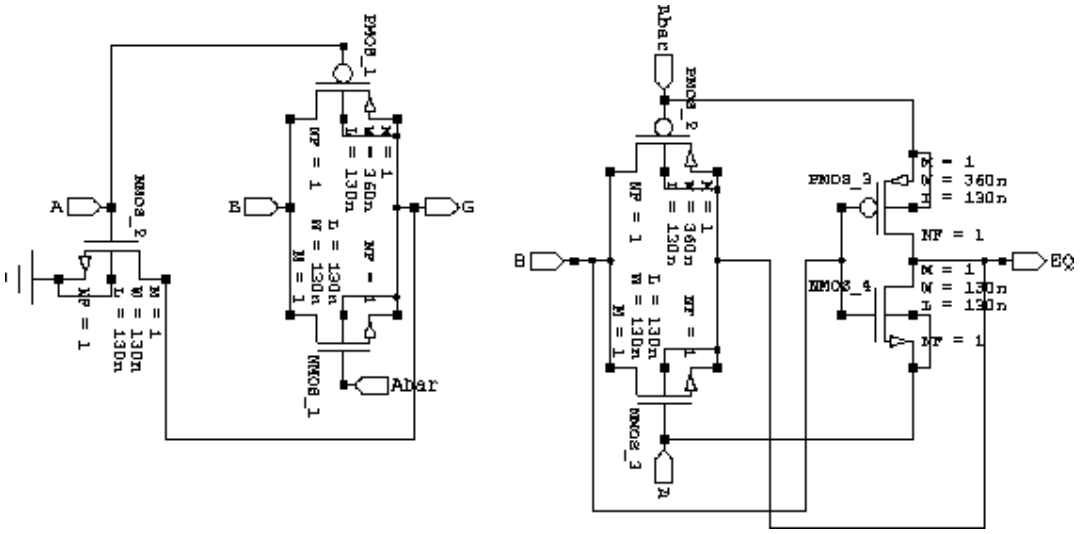
$$G_{[i]} = \overline{A_{[i]}}B_{[i]}; EQ_{[i]} = \overline{A_{[i]} \oplus B_{[i]}} \quad (4)$$

where i=0..... 63.
The equation (1) and (2) can then be simplified to

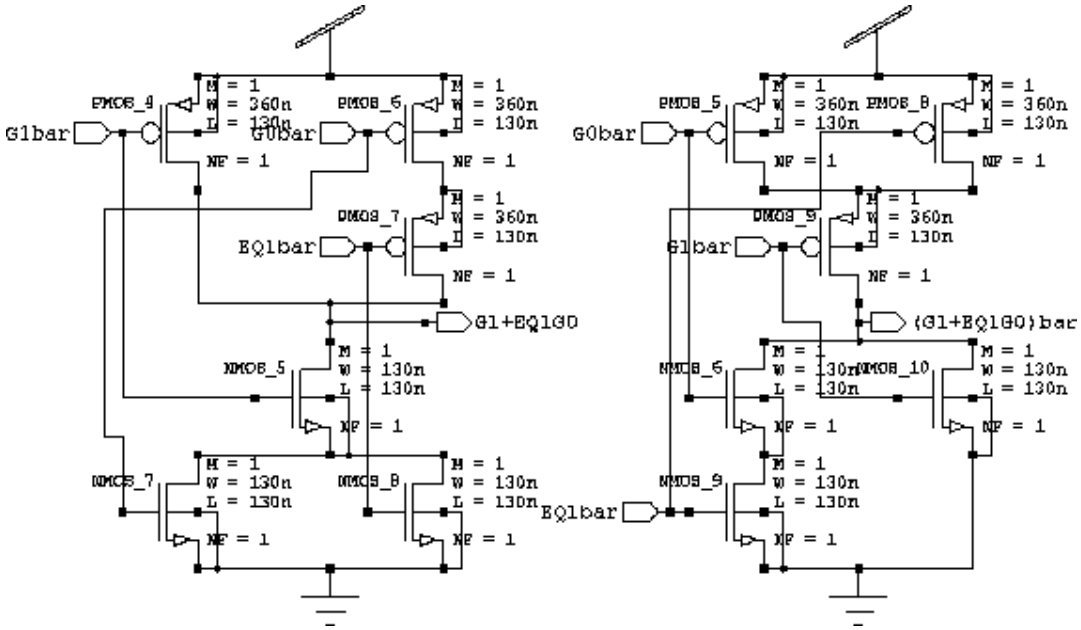
$$B_{Big[2j+1:2j]} = G_{[2j+1]} + EQ_{[2j+1]}G_{[2j]} \quad (5)$$

$$EQ_{[2j+1:2j]} = EQ_{[2j+1]}.EQ_{[2j]} \quad (6)$$

where j=0..... 31.



(a)



(b)

Figure 3. Schematics of (a) pre-encode and (b) comparison generation.

The G and P signals can be further combined to form group G and P signals, i.e.,

$$B_{Big[3:0]} = \overline{A_3}B_3 + \left(A_3 \oplus B_3\right).\left\{\overline{A_2}B_2 + \left(A_2 \oplus B_2\right)\left[\overline{A_1}B_1 + \left(\overline{A_1 \oplus B_1}\right)\left(\overline{A_0}B_0\right)\right]\right\}$$
$$= G_3 + EQ_3\left(G_2 + EQ_2\left(G_1 + EQ_1C_{in}\right)\right)$$
$$= B_{Big[3:2]} + EQ_{[3:2]}B_{Big[1:0]}$$

Finally, the 64-bit comparator can be obtained by using the equations

$$B_{Big[63:0]} = G_{63} + \sum_{k=0}^{62}\left(G_k \cdot \prod_{m=k+1}^{63} EQ_m\right)$$

$$EQ_{[63:0]} = \prod_{m=0}^{63} EQ_m$$

Figure 3 shows the schematic diagram of pre-encoder and comparison generation circuit. Pass transistor logic is used in pre-encoding circuit and it reduces the number of transistors, which optimizes the energy. CMOS logic is used in comparison generation circuit and is optimized for PDP; hence static logic is employed to facilitate high-performance low-power operations.

IV. SIMULATION AND POWER RESULTS

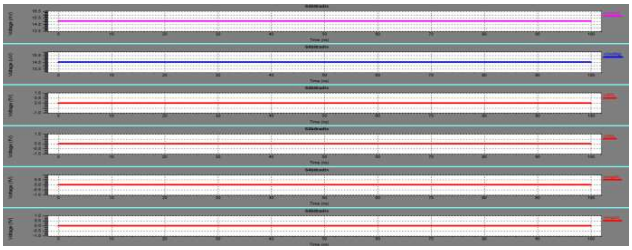


Figure 4. A>B

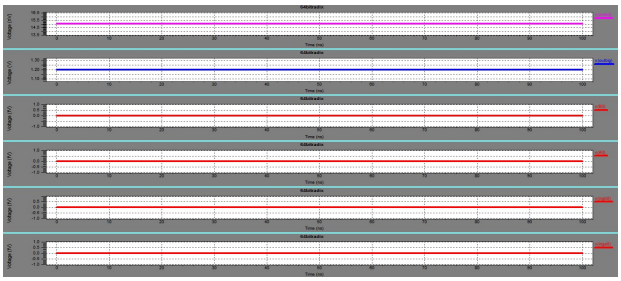


Figure 5. A<B

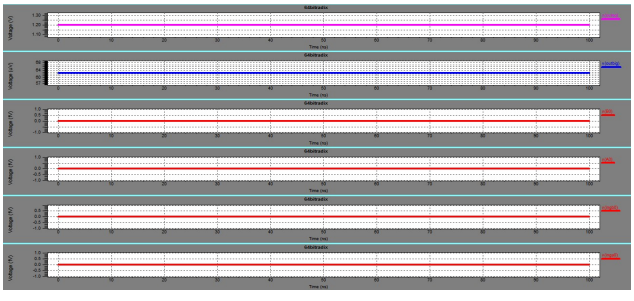


Figure 6. A=B

TABLE I

Power Comparison

Condition	Exiting Comparator (mW)	Proposed Comparator (mW)
A>B	48.21	3.35
A<B	48.08	3.31
A=B	43.42	3.25

Table I shows the comparison between the Existing comparator and the proposed comparator and power has been reduced in the proposed comparator.

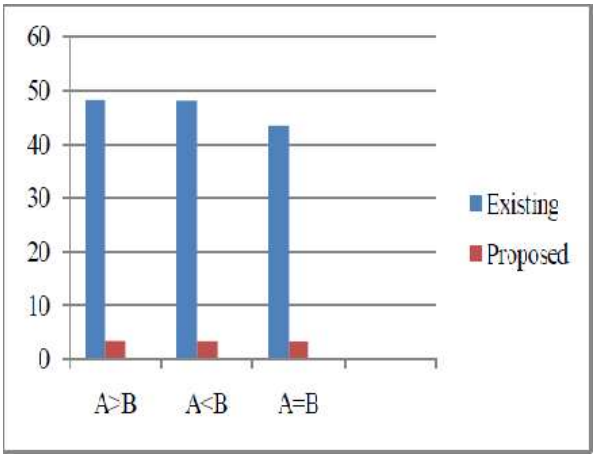


Figure 7. Power result comparison of existing and proposed comparators

V. CONCLUSION

A new 64-bit static logic binary comparator has been designed. In this design, pre-encoding circuitry is used which is optimized for energy and helps to reduce the number of transistors. Pass transistor logic is used to reduce the number of transistors. It also involves the usage of comparison generation circuitry which optimizes the power delay product. This design gives low-power high-performance operations, as compared with existing designs. Hence by using static logic binary comparator, the power has been reduced in the proposed comparator.

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